PCI-SIG ENGINEERING CHANGE NOTICE

TITLE:	Surprise Down Error & Link Up Additions
DATE:	4 Feb 2004 (updated 10 June 2004)
AFFECTED DOCUMENT:	PCI Express Base Specification Revision 1.0a
SPONSOR:	David Harriman, Intel Corporation

Part I

1. Summary of the Functional Changes

This document proposes a new optional error detection & logging/reporting capability for "Surprise Down" type errors. Such an error exists when a link goes from up (L0/DL_Active) to down (Detect/DL_Inactive) unexpectedly, for example, in a case where such a transition is not supported by hot plug (for the affected link).

In addition, a bit is added to report Link Up (Data Link Layer DL_Active) state.

Note that this document comprehends preceding errata.

2. Benefits as a Result of the Changes

Improves error reporting capabilities through optional new capability.

3. Assessment of the Impact

No negative impact. New optional capabilities.

4. Analysis of the Hardware Implications

No negative impact. New optional capabilities – builds on existing infrastructure such that implementation, if desired, should be straightforward.

5. Analysis of the Software Implications

Software that does not comprehend the new error type will still be able to control the reporting mechanism using the fatal error reporting control infrastructure, but will not be able to control the specific error in Advanced Error Handling. New software should be written to comprehend this new optional capability.

Part II

Detailed Description of the change

In 3.2.1 Data Link Control and Management State Machine Rules:

...

- DL_Active

...

- Exit to DL_Inactive if:
  - Physical Layer reports Physical LinkUp = 0
  - Upstream components are optionally permitted to treat this transition from DL_Active to DL_Inactive as a Surprise Down error, with the following exceptions:

    * If the Secondary Bus Reset in Bridge Control Register has been set to 1b by software, then the subsequent transition to DL_Inactive must not be considered an error.

    * If the Link Disable bit has been set to 1b by software, then the subsequent transition to DL_Inactive must not be considered an error.

    * If a PME_Turn_Off Message has been sent through this port, then the subsequent transition to DL_Inactive must not be considered an error.

    * If the port is associated with a hot-pluggable slot, and the Hot Plug Surprise bit in the Slot Capabilities Register is set to 1b, then any transition to DL_Inactive must not be considered an error.

    * If the port is associated with a hot-pluggable slot (Hot-Plug Capable bit in the Slot Capabilities Register set to 1b), and Power Controller Control bit in Slot Control Register is 1b(Off), then any transition to DL Inactive must not be considered an error.

    If the error is masked by any of the above exceptions, either of the following events must cause error unmasking:

    * A transition to DL_Inactive

    * The successful reception and forwarding to the Receive Transaction Layer (see Section 3.5.3.1) of any TLP

    If implemented, this is a reported error associated with the detecting port (see Section 6.2).

In 6.2.6. Error Listing and Rules:

...

Table 6-3: Data Link Layer Error List

Error Name	Severity	Detecting Agent Action[xx]
Bad TLP	Correctable	*Receiver:* Send ERR_COR to Root Complex.
Bad DLLP		*Receiver:* Send ERR_COR to Root Complex.
Replay Timeout		*Transmitter:* Send ERR_COR to Root Complex.
REPLAY NUM Rollover		*Transmitter:* Send ERR_COR to Root Complex.
Data Link Layer Protocol Error	Uncorrectable (Fatal)	If checking, send ERR_FATAL to Root Complex.
Surprise Down		If checking, send ERR_FATAL to Root Complex.

In 7.8.6, Link Capabilities Register:

...

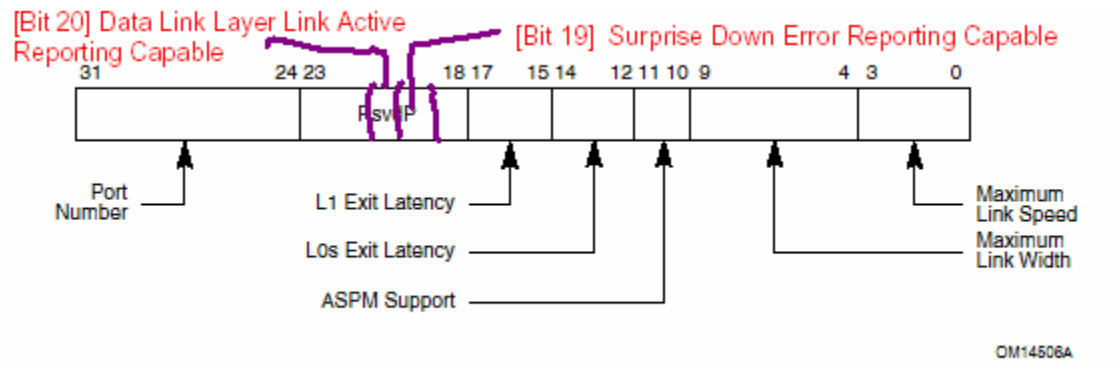

Figure 7-16: Link Capabilities Register

Table 7-14: Link Capabilities Register

Bit Location	Register Description	Attributes
...		
17:15	**...**	
19	**Surprise Down Error Reporting Capable –** For a Downstream Port, this bit must be set to 1b if the component supports the optional capability of detecting and reporting a Surprise Down error condition. For Upstream Ports and components that do not support this optional capability, this bit must be hardwired to 0b.	RO

Bit Location	Register Description	Attributes
20	**Data Link Layer Link Active Reporting Capable –** For a Downstream Port, this bit must be set to 1b if the component supports the optional capability of reporting the DL_Active state of the Data Link Control and Management State Machine. For Upstream Ports and components that do not support this optional capability, this bit must be hardwired to 0b.	RO
31:24	...	

Ed. Note: The earlier version of this ECN had added a "Surprise Down Reporting Enable" bit, which has been removed from this version. This error doesn't need an independent control & the existence of this bit is confusing/conflicting w.r.t. control in the AER structure

In 7.8.8, Link Status Register (note: preceding ECN removing Training Error reflected in the markups below):

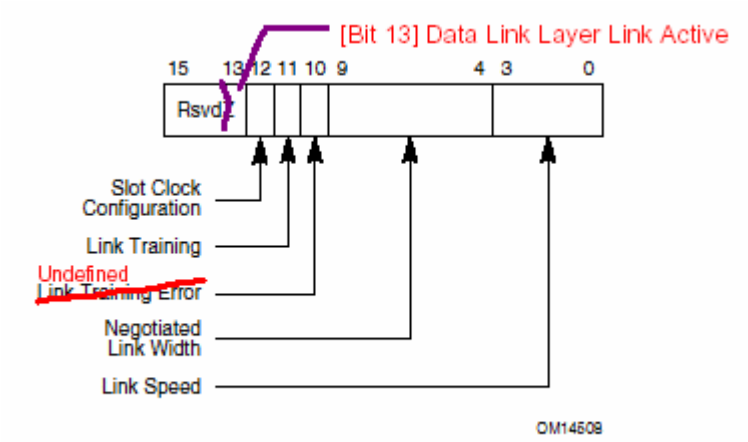

Figure 7-18: Link Status Register

Table 7-16: Link Status Register

Bit Location	Register Description	Attributes
...		
13	**Data Link Layer Link Active** (Optional) – Set to 1b when the Data Link Control and Management State Machine is in the DL_Active state, 0b otherwise. If this optional status reporting capability is not implemented, this bit must be hardwired to 0b.	RO

In 7.10.2, Uncorrectable Error Status Register (note: preceding ECN removing Training Error reflected in the markups below):

...

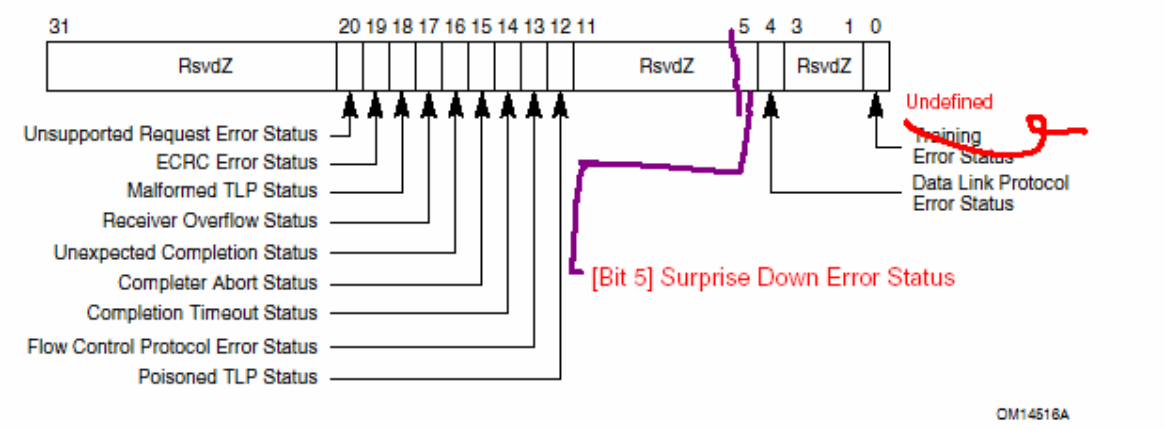

Figure 7-28: Uncorrectable Error Status Register

Table 7-24: Uncorrectable Error Status Register

Bit Location	Register Description	Attributes	Default Value
...			
5	**Surprise Down Error Status** (Optional)	RW1CS	0
...			

In 7.10.3, Uncorrectable Error Mask Register (note: preceding ECN removing Training Error reflected in the markups below):

...

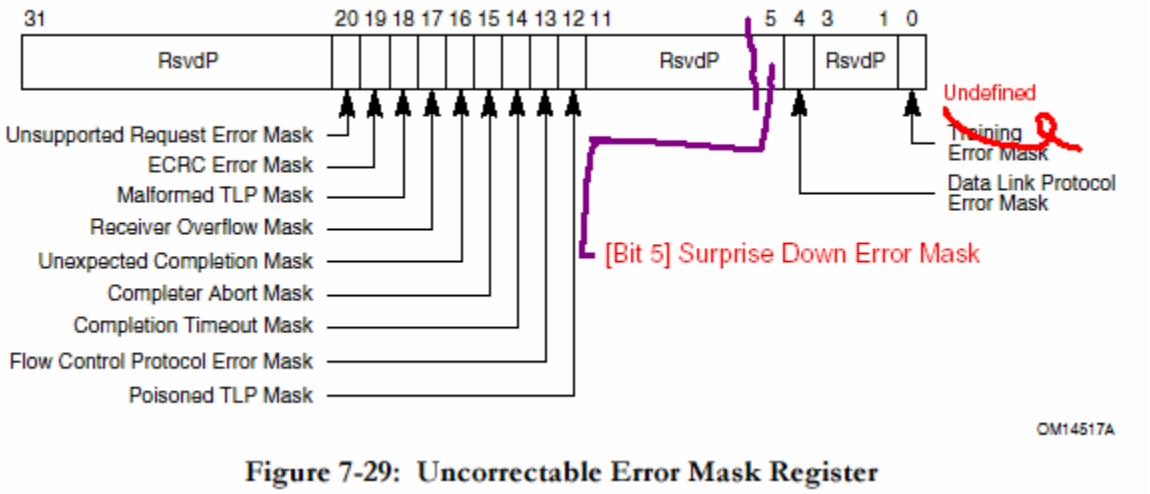

Figure 7-29: Uncorrectable Error Mask Register

Table 7-25: Uncorrectable Error Mask Register

Bit Location	Register Description	Attributes	Default Value
...			
5	**Surprise Down Error Mask** (Optional)	RWS	0
...			

In 7.10.4, Uncorrectable Error Severity Register (note: preceding ECN removing Training Error reflected in the markups below):

...

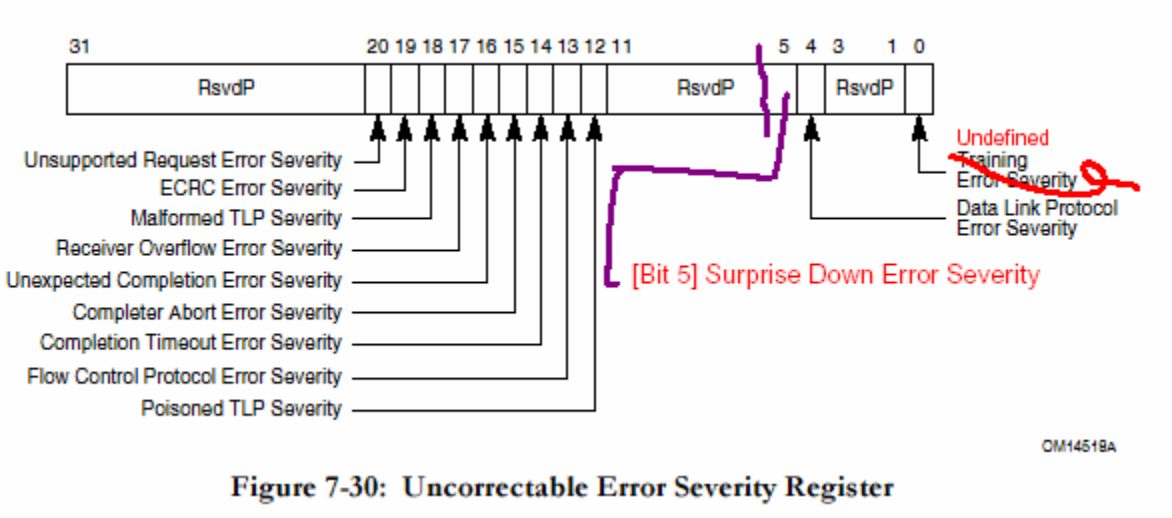

Figure 7-30: Uncorrectable Error Severity Register

Table 7-26: Uncorrectable Error Severity Register

Bit Location	Register Description	Attributes	Default Value
...			
5	**Surprise Down Error Severity** (Optional)	RWS	1
...			

-- end of change --